Data Sheet | January 17, 2006 | FN9210.2

TFT-LCD Power Supply

The EL7586 and EL7586A represent multiple output regulators for use in all large panel, TFT-LCD applications. Both feature a single boost converter with an integrated 2A FET, two positive LDOs for V_{ON} and V_{LOGIC} generation, and a single negative LDO for V_{OFF} generation. The boost converter can be programmed to operate in either P-mode or PI-mode for improved load regulation.

Both EL7586 and EL7586A also integrate fault protection for all four channels. Once a fault is detected, the device is latched off until the input supply or EN is cycled. EL7586 also features an integrated start-up sequence for V_{BOOST}/V_{LOGIC}, V_{OFF}, then V_{ON} or for V_{LOGIC}, V_{OFF}, V_{BOOST}, and V_{ON}. The latter requires a single external transistor. The timing of the start-up sequence is set using an external capacitor.

EL7586A features an immediately-enabled V_{LOGIC} output which is independent of EN input. The V_{LOGIC} output will be switched off if a fault is detected and the power supply needs to be recycled to reset this condition.

Both the EL7586 and EL7586A are pin-compatible, come in the 20 Ld 4x4 QFN package, and are specified for operation over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL7586ILZ (Note)	7586ILZ	-	20 Ld 4x4 QFN (Pb-free)	MDP0046
EL7586ILZ-T7 (Note)	7586ILZ	7”	20 Ld 4x4 QFN (Pb-free)	MDP0046
EL7586ILZ-T13 (Note)	7586ILZ	13”	20 Ld 4x4 QFN (Pb-free)	MDP0046
EL7586AILZ (Note)	7586AIL Z	-	20 Ld 4x4 QFN (Pb-free)	MDP0046
EL7586AILZ-T7 (Note)	7586AIL Z	7”	20 Ld 4x4 QFN (Pb-free)	MDP0046
EL7586AILZ-T13 (Note)	7586AIL Z	13”	20 Ld 4x4 QFN (Pb-free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

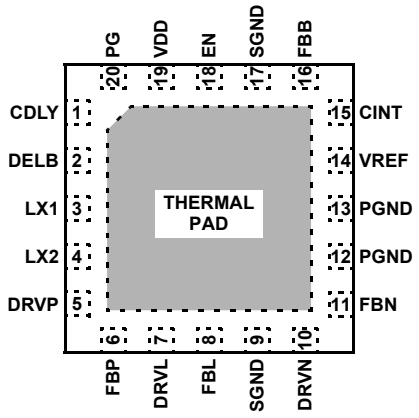
- 2A current limit FET options
- 3V to 5V input
- Up to 20V boost out
- 1% regulation on all outputs
- V_{LOGIC}-V_{OFF}-V_{BOOST}-V_{ON} or V_{BOOST}/V_{LOGIC}-V_{OFF}-V_{ON} sequence control
  - V_{LOGIC} is on from start-up for EL7586A
- Programmable sequence delay
- Fully fault protected
- Thermal shutdown
- Internal soft-start
- 20 Ld 4x4 QFN packages
- Pb-free plus anneal available (RoHS compliant)

Applications

- LCD monitors (15”+)
- LCD-TV (up to 40”+)
- Notebook displays (up to 16”)
- Industrial/medical LCD displays

Pinout

EL7586, EL7586A
(20 LD 4X4 QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_{DELB} 24V
V_{DRVP} 36V
V_{DRVN} . . . . . -20V
V_{DD} 6.5V
V_{LX} 24V
V_{DRVL} 6.5V
Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves
Maximum Continuous Junction Temperature . . . . . 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, over temperature from -40°C to 85°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
V_S	Supply Voltage		3		5.5	V
I_S	Quiescent Current (EL7586A)	Enabled, LX not switching		1.7	2.5	mA
		Disabled		750	900	µA
I_S	Quiescent Current (EL7586)	Enabled, LX not switching		1.7	2.5	mA
		Disabled		10	20	µA
CLOCK						
F_{OSC}	Oscillator Frequency		900	1000	1100	kHz
BOOST						
V_{BOOST}	Boost Output Range		5.5		20	V
V_{FBB}	Boost Feedback Voltage	T_A = 25°C	1.192	1.205	1.218	V
			1.188	1.205	1.222	V
V_{F_FBB}	FBB Fault Trip Point			0.9		V
V_{REF}	Reference Voltage	T_A = 25°C	1.19	1.215	1.235	V
			1.187	1.215	1.238	V
C_{REF}	V_{REF} Capacitor		22	100		nF
D_{MAX}	Maximum Duty Cycle		85			%
I_{LXMAX}	Current Switch			2.0		A
I_{LEAK}	Switch Leakage Current	V_{LX} = 16V			10	µA
$r_{DS(ON}$	Switch On-Resistance			320		mΩ
Eff	Boost Efficiency	See curves	85	92		%
$I(V_{FBB})$	Feedback Input Bias Current	PI mode, V_{FBB} = 1.35V		50	500	nA
$\Delta V_{BOOST}/\Delta V_{IN}$	Line Regulation	C_{INT} = 4.7nF, I_{OUT} = 100mA, V_{IN} = 3V to 5.5V		0.05		%/V
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - "P" Mode	C_{INT} pin strapped to V_{DD}, 50mA < I_{LOAD} < 250mA		3		%
$\Delta V_{BOOST}/\Delta I_{BOOST}$	Load Regulation - "PI" Mode	C_{INT} = 4.7nF, 50mA < I_O < 250mA		0.1		%
V_{CINT_T}	CINT PI Mode Select Threshold			4.7	4.8	V

Electrical Specifications V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, over temperature from -40°C to 85°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
V_{ON} LDO						
V_{FBP}	FBP Regulation Voltage	I_{DRVP} = 0.2mA, T_A = 25°C	1.176	1.2	1.224	V
		I_{DRVP} = 0.2mA	1.172	1.2	1.228	V
V_{F_FBP}	FBP Fault Trip Point	V_{FBP} falling	0.82	0.87	0.92	V
I_{FBP}	FBP Input Bias Current	V_{FBP} = 1.35V	-250		250	nA
GMP	FBP Effective Transconductance	V_{DRVP} = 25V, I_{DRVP} = 0.2 to 2mA		50		ms
$\Delta V_{ON}/\Delta I(V_{ON})$	V_{ON} Load Regulation	$I(V_{ON})$ = 0mA to 20mA		-0.5		%
I_{DRVP}	DRVP Sink Current Max	V_{FBP} = 1.1V, V_{DRVP} = 25V	2	4		mA
I_{L_DRVP}	DRVP Leakage Current	V_{FBP} = 1.5V, V_{DRVP} = 35V		0.1	5	µA
V_{OFF} LDO						
V_{FBN}	FBN Regulation Voltage	I_{DRVN} = 0.2mA, T_A = 25°C	0.173	0.203	0.233	V
		I_{DRVN} = 0.2mA	0.171	0.203	0.235	V
V_{F_FBN}	FNN Fault Trip Point	V_{FBN} falling	0.38	0.43	0.48	V
I_{FBN}	FBN Input Bias Current	V_{FBN} = 0.2V	-250		250	nA
GMN	FBN Effective Transconductance	V_{DRVN} = -6V, I_{DRVN} = 0.2mA to 2mA		50		ms
$\Delta V_{OFF}/\Delta I(V_{OFF})$	V_{OFF} Load Regulation	$I(V_{OFF})$ = 0mA to 20mA		-0.5		%
I_{DRVN}	DRVN Source Current Max	V_{FBN} = 0.3V, V_{DRVN} = -6V	2	4		mA
I_{L_DRVN}	DRVN Leakage Current	V_{FBN} = 0V, V_{DRVN} = -20V		0.1	5	µA
V_{LOGIC} LDO						
V_{FBL}	FBL Regulation Voltage	I_{DRVL} = 1mA, T_A = 25°C	1.176	1.2	1.224	V
		I_{DRVL} = 1mA	1.174	1.2	1.226	V
V_{F_FBL}	FBL Fault Trip Point	V_{FBL} falling	0.82	0.87	0.92	V
I_{FBL}	FBL Input Bias Current	V_{FBL} = 1.35V	-500		500	nA
G_{ML}	FBL Effective Transconductance	V_{DRVL} = 2.5V, I_{DRVL} = 1mA to 8mA		200		ms
$\Delta V_{LOGIC}/\Delta I(V_{LOGIC})$	V_{LOGIC} Load Regulation	$I(V_{LOGIC})$ = 100mA to 500mA		0.5		%
I_{DRVL}	DRVL Sink Current Max	V_{FBL} = 1.1V, V_{DRVL} = 2.5V	8	16		mA
I_{L_DRL}	I_{L_DRVL}	V_{FBL} = 1.5V, V_{DRVL} = 5.5V		0.1	5	µA
SEQUENCING						
t_{ON}	Turn On Delay	C_{DLY} = 0.22µF		30		ms
t_{SS}	Soft-start Time	C_{DLY} = 0.22µF		2		ms
t_{DEL1}	Delay Between A_{VDD} and V_{OFF}	C_{DLY} = 0.22µF		10		ms
t_{DEL2}	Delay Between V_{ON} and V_{OFF}	C_{DLY} = 0.22µF		17		ms
I_{DELB}	DELB Pull-down Current	V_{DELB} > 0.6V		50		µA
		V_{DELB} < 0.6V		1.4		mA
C_{DEL}	Delay Capacitor		10	220		nF

Electrical Specifications V_{DD} = 5V, V_{BOOST} = 11V, I_{LOAD} = 200mA, V_{ON} = 15V, V_{OFF} = -5V, V_{LOGIC} = 2.5V, over temperature from -40°C to 85°C, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
FAULT DETECTION						
t_{FAULT}	Fault Time Out	C_{DLY} = 0.22µF		50		ms
OT	Over-temperature Threshold			140		°C
I_{PG}	PG Pull-down Current	VPG > 0.6V		15		µA
		VPG < 0.6V		1.7		mA
LOGIC ENABLE						
V_{HI}	Logic High Threshold		2.3			V
V_{LO}	Logic Low Threshold				0.8	V
I_{LOW}	Logic Low Bias Current			0.2	2	µA
I_{HIGH}	Logic High Bias Current	at V_{EN} = 5V	12	18	24	µA

Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
1	CDLY	A capacitor connected from this pin to GND sets the delay time for start-up sequence and sets the fault timeout time
2	DELB	Open drain output for gate drive of optional V_{BOOST} delay FET
3, 4	LX1, LX2	Drain of the internal N channel boost FET; for EL7586, pin 4 is not connected
5	DRVP	Positive LDO base drive; open drain of an internal N channel FET
6	FBP	Positive LDO voltage feedback input pin; regulates to 1.2V nominal
7	DRVL	Logic LDO base drive; open drain of an internal N channel FET
8	FBL	Logic LDO voltage feedback input pin; regulates to 1.2V nominal
9, 17	SGND	Low noise signal ground
10	DRVN	Negative LDO base drive; open drain of an internal P channel FET
11	FBN	Negative LDO voltage feedback input pin; regulates to 0.2V nominal
12, 13	PGND	Power ground, connected to source of internal N channel boost FET
14	VREF	Bandgap voltage bypass, connect a 0.1µF to SGND
15	CINT	V_{BOOST} integrator output, connect capacitor to SGND for PI mode or connect to V_{DD} for P mode operation
16	FBB	Boost regulator voltage feedback input pin; regulates to 1.2V nominal
18	EN	Enable pin, High = Enable; Low or floating = Disable
19	VDD	Positive supply
20	PG	Push-pull gate drive of optional fault protection FET, when chip is disabled or when a fault has been detected, this is high

Typical Performance Curves

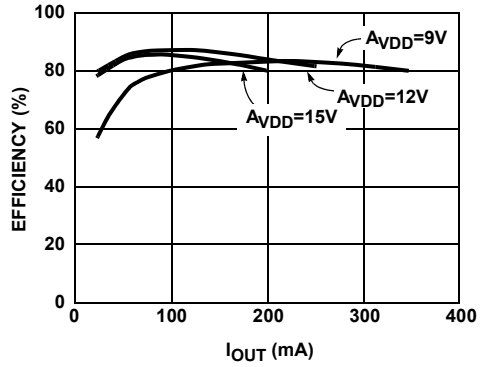


FIGURE 1. V_{BOOST} EFFICIENCY AT V_{IN} = 3V (PI MODE)

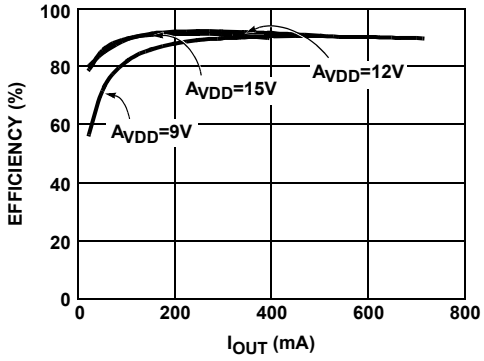


FIGURE 2. V_{BOOST} EFFICIENCY AT V_{IN} = 5V (PI MODE)

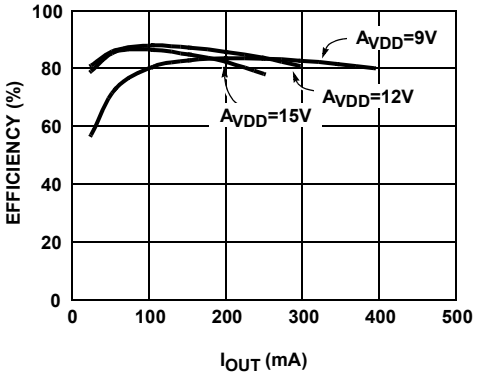


FIGURE 3. V_{BOOST} EFFICIENCY AT V_{IN} = 3V (P MODE)

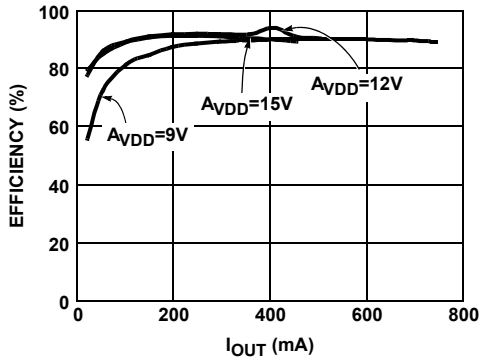


FIGURE 4. V_{BOOST} EFFICIENCY AT V_{IN} = 5V (P MODE)

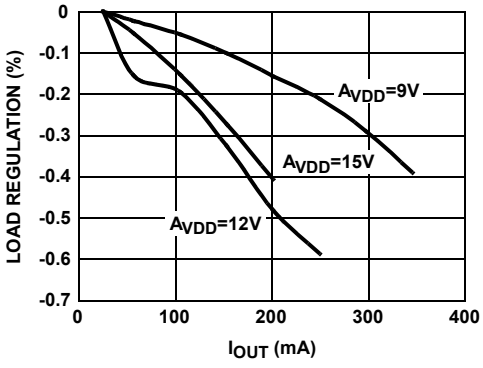


FIGURE 5. V_{BOOST} LOAD REGULATION AT V_{IN} = 3V (PI MODE)

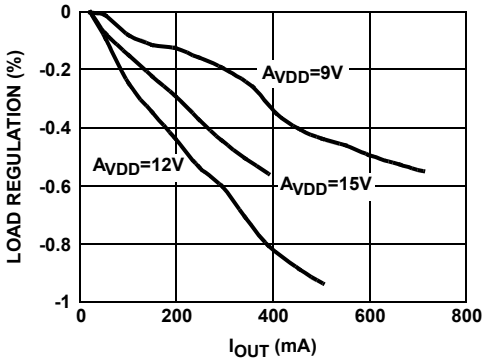


FIGURE 6. V_{BOOST} LOAD REGULATION AT V_{IN} = 5V (PI MODE)

Typical Performance Curves (Continued)

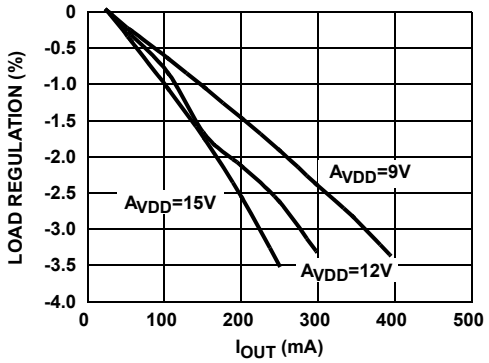


FIGURE 7. V_{BOOST} LOAD REGULATION AT V_{IN} = 3V (P MODE)

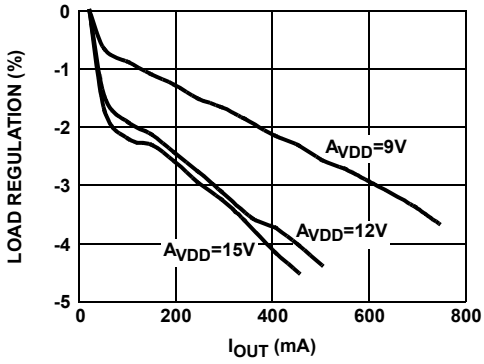


FIGURE 8. V_{BOOST} LOAD REGULATION AT V_{IN} = 5V (P MODE)

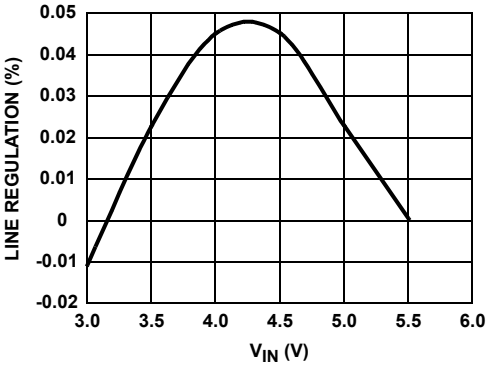


FIGURE 9. V_{BOOST} LINE REGULATION (PI MODE)

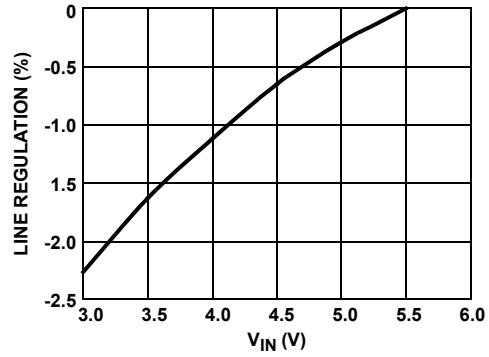


FIGURE 10. V_{BOOST} LINE REGULATION (P MODE)

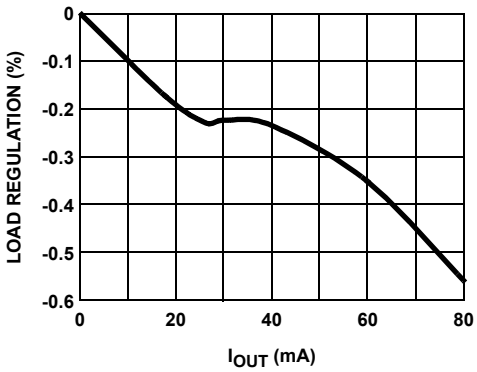


FIGURE 11. V_{ON} LOAD REGULATION

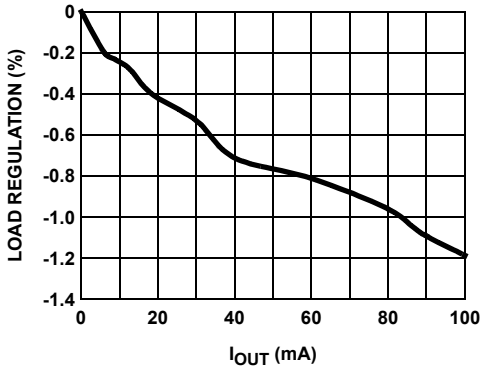


FIGURE 12. V_{OFF} LOAD REGULATION

Typical Performance Curves (Continued)

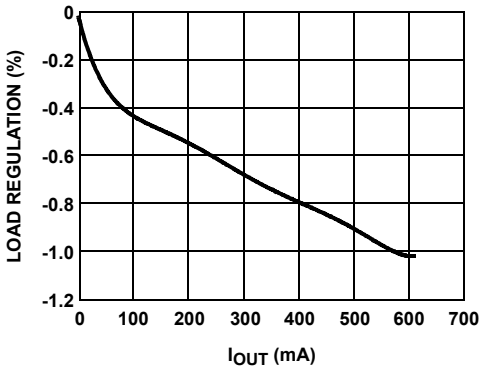


FIGURE 13. V_{LOGIC} LOAD REGULATION

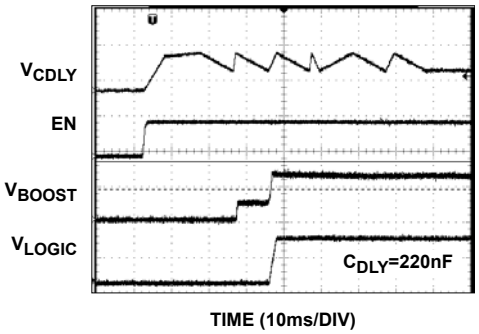


FIGURE 14. EL7586 START-UP SEQUENCE

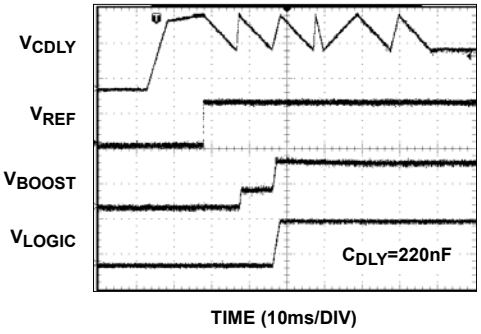


FIGURE 15. EL7586 START-UP SEQUENCE

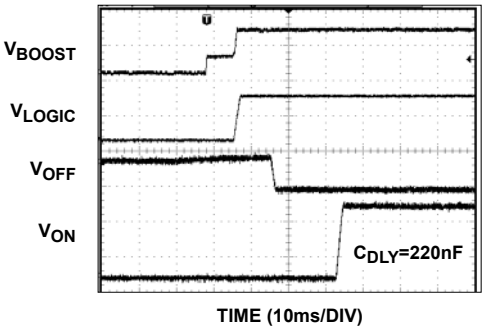


FIGURE 16. EL7586 START-UP SEQUENCE

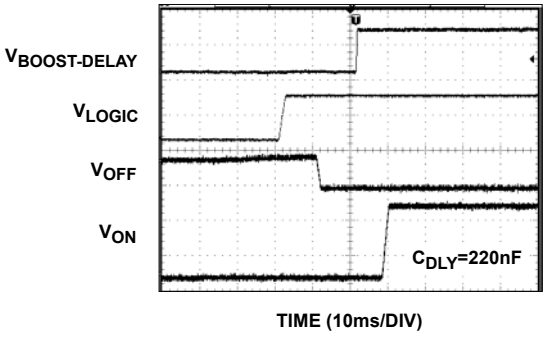


FIGURE 17. EL7586 START-UP SEQUENCE

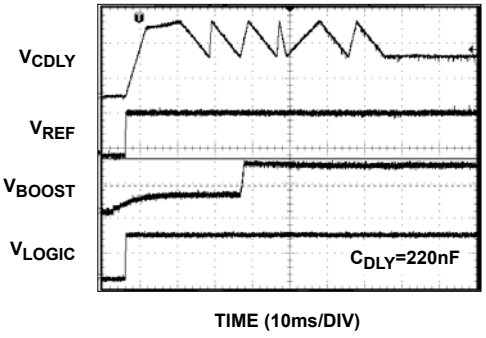


FIGURE 18. EL7586A START-UP SEQUENCE

Typical Performance Curves (Continued)

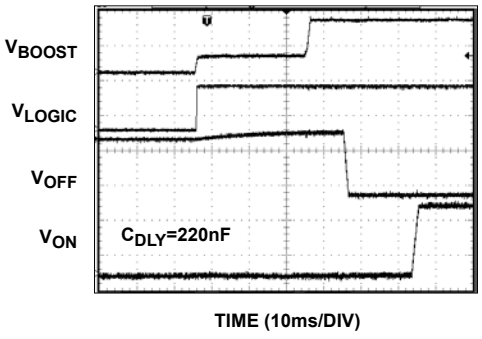


FIGURE 19. EL7586A START-UP SEQUENCE

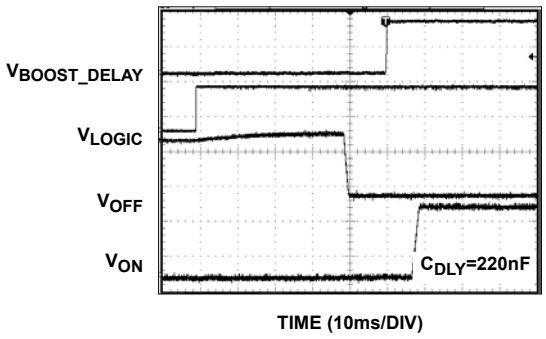


FIGURE 20. EL7586A START-UP SEQUENCE

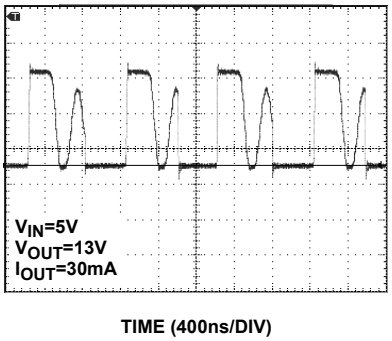


FIGURE 21. LX WAVEFORM - DISCONTINUOUS MODE

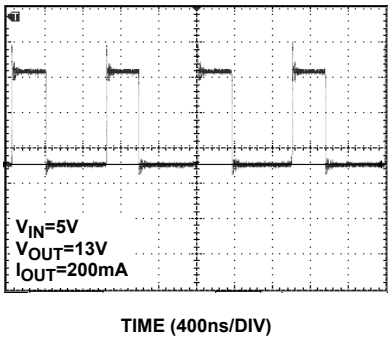


FIGURE 22. LX WAVEFORM - CONTINUOUS MODE

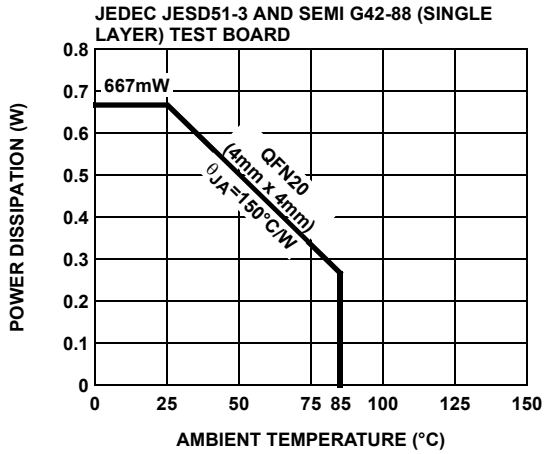


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

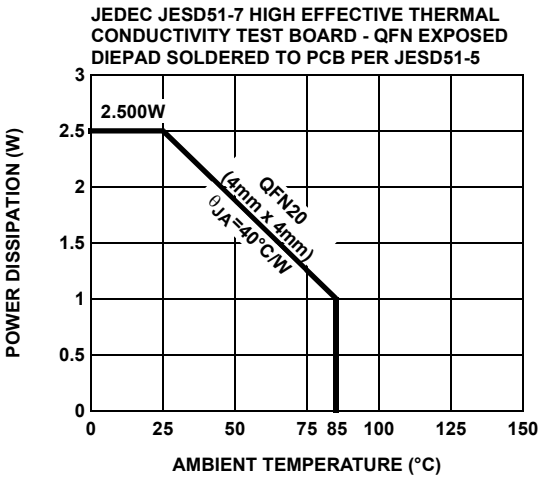


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The EL7586 and EL7586A provide a high integrated multiple output power solution for TFT-LCD applications. The system consists of one high efficiency boost converter and three linear-regulator controllers (V_{ON}, V_{OFF}, and V_{LOGIC}) with multiple protection functions. A block diagram is shown in Figure 25. Table 1 lists the recommended components.

The EL7586, and EL7586A integrate an N-channel MOSFET boost converter to minimize external component count and cost. The A_{VDD}, V_{ON}, V_{OFF}, and V_{LOGIC} output voltages are independently set using external resistors. V_{ON}, V_{OFF} voltages require external charge pumps which are post regulated using the integrated LDO controllers.

TABLE 1. RECOMMENDED COMPONENTS

DESIGNATION	DESCRIPTION
C_1, C_2, C_3	10µF, 16V X7R ceramic capacitor (1206) TDK C3216X7RIC106M
C_{20}, C_{31}	4.7µF, 25V X5R ceramic capacitor (1206) TDK C3216X5R1A475K
D_1	1A 20V low leakage Schottky rectifier (CASE 457-04) ON SEMI MBRM120ET3
D_{11}, D_{12}, D_{21}	200mA 30V Schottky barrier diode (SOT-23) Fairchild BAT54S
L_1	6.8µH 1.3A Inductor TDK SLF6025T-6R8M1R3-PF
Q_1	-2.4 -20V P-channel 1.8V specified PowerTrench MOSFET (SuperSOT-3) Fairchild FDN304P
Q_4	-2A -30V single P-channel logic level PowerTrench MOSFET (SuperSOT-3) Fairchild FDN360P
Q_3	200mA 40V PNP amplifier (SOT-23) Fairchild MMBT3906
Q_2	200mA 40V NPN amplifier (SOT-23) Fairchild MMBT3904
Q_5	1A 30V PNP low saturation amplifier (SOT-23) Fairchild FMMT549

Boost Converter

The main boost converter is a current mode PWM converter at a fixed frequency of 1MHz which enables the use of low profile inductors and multiplayer ceramic capacitors. This results in a compact, low cost power system for LCD panel design.

The EL7586 and EL7586A are designed for continuous current mode, but they can also operate in discontinuous current mode at light load. In continuous current mode, current flows continuously in the inductor during the entire switching cycle in steady state operation. The voltage conversion ratio in continuous current mode is given by:

$$\frac{A_{VDD}}{V_{IN}} = \frac{1}{1-D}$$

Where D is the duty cycle of the switching MOSFET.

Figure 26 shows the block diagram of the boost regulator. It uses a summing amplifier architecture consisting of GM stages for voltage feedback, current feedback and slope compensation. A comparator looks at the peak inductor current cycle by cycle and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network in the order of 60kΩ is recommended. The boost converter output voltage is determined by the following equation:

$$A_{VDD} = \frac{R_1 + R_2}{R_1} \times V_{REF}$$

The current through the MOSFET is limited to 2A peak for the EL7586. This restricts the maximum output current based on the following equation:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O}$$

Where ΔIL is peak to peak inductor ripple current, and is set by:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_S}$$

where f_S is the switching frequency.

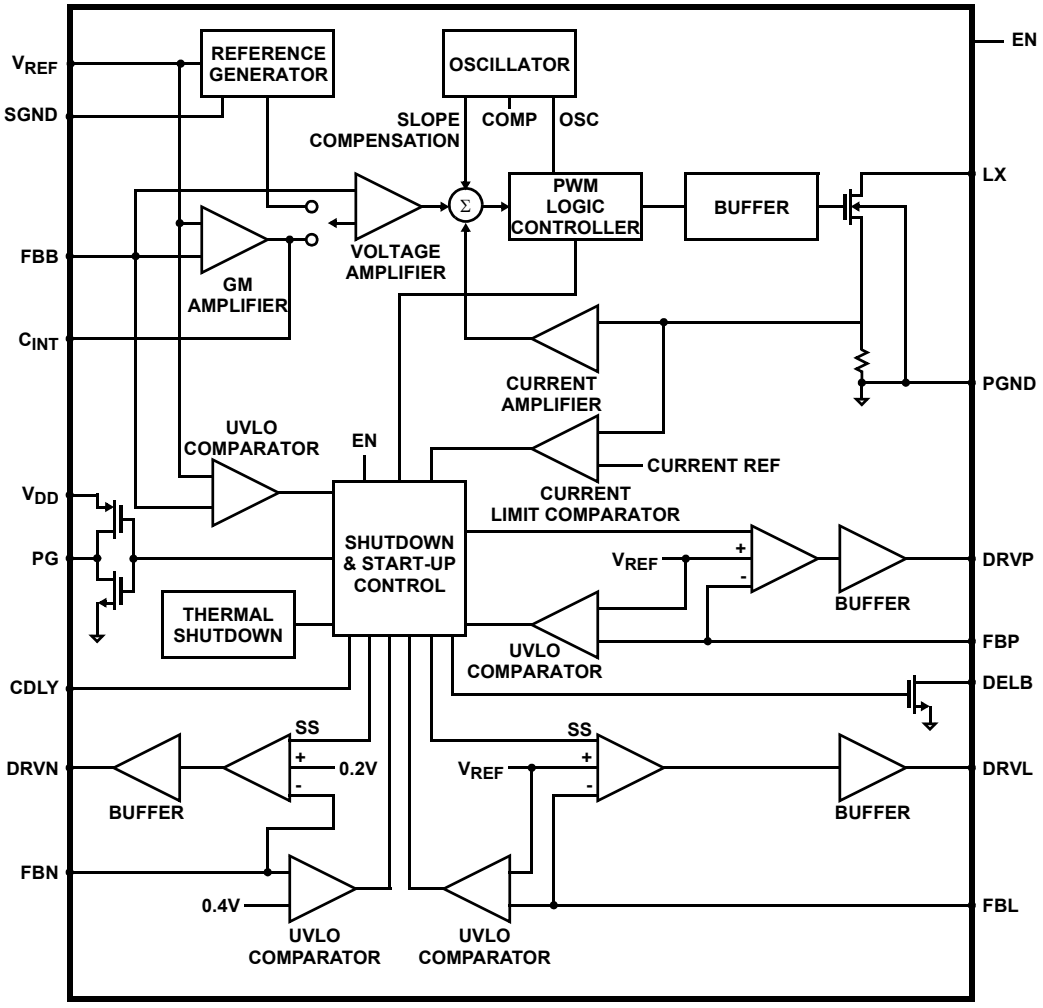


FIGURE 25. BLOCK DIAGRAM

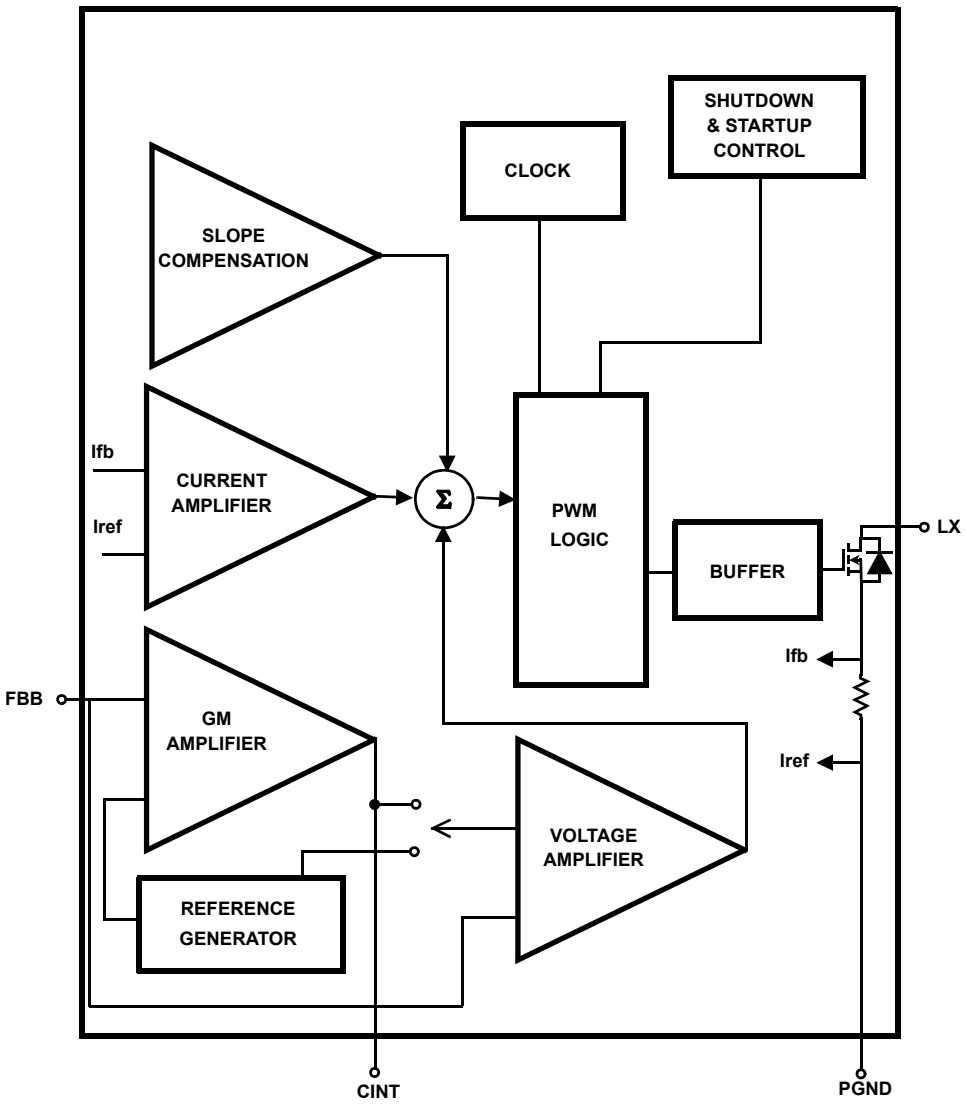


FIGURE 26. BLOCK DIAGRAM OF THE BOOST REGULATOR

The following table gives typical values (margins are considered 10%, 3%, 20%, 10%, and 15% on V_{IN}, V_O, L, f_S, and I_{OMAX}:

TABLE 2.

V_{IN} (V)	V_O (V)	L (µH)	f_S (MHz)	I_{OMAX} (EL7586, EL7586A)
3.3	9	6.8	1	0.490686
3.3	12	6.8	1	0.307353
3.3	15	6.8	1	0.197353
5	9	6.8	1	0.743464
5	12	6.8	1	0.465686
5	15	6.8	1	0.29902

Input Capacitor

An input capacitor is used to supply the peak charging current to the converter. It is recommended that C_{IN} be larger than 10µF. The reflected ripple voltage will be smaller with larger C_{IN}. The voltage rating of input capacitor should be larger than maximum input voltage.

Boost Inductor

The boost inductor is a critical part which influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are to match the internal slope compensation. The inductor must be able to handle the following average and peak current:

$$I_{LAVG} = \frac{I_O}{1-D}$$

$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2}$$

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The rectifier diode must meet the output current and peak inductor current requirements.

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components: the voltage drop due to the inductor ripple current flowing through the ESR of output capacitor, and the charging and discharging of the output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_S}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

NOTE: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in the equation above assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at zero volts.

Compensation

The EL7586, and EL7586A can operate in either P mode or PI mode. Connecting the C_{INT} pin directly to V_{IN} will enable P mode; For better load regulation, use PI mode with a 4.7nF capacitor in series with a 10K resistor between C_{INT} and ground. This value may be reduced to improve transient performance, however, very low values will reduce loop stability.

Boost Feedback Resistors

As the boost output voltage, A_{VDD}, is reduced below 12V the effective voltage feedback in the IC increases the ratio of voltage to current feedback at the summing comparator because R_2 decreases relative to R_1. To maintain stable operation over the complete current range of the IC, the voltage feedback to the FBB pin should be reduced proportionally, as A_{VDD} is reduced, by means of a series resistor-capacitor network (R_7 and C_7) in parallel with R_1, with a pole frequency (f_p) set to approximately 10kHz for C_2 effective = 10µF and 4kHz for C_2 (effective) = 30µF.

$R_7 = ((1/0.1 \times R_2) - 1/R_1)^{-1}$

$C_7 = 1/(2 \times 3.142 \times f_p \times R_7)$

PI Mode C_{INT} (C_{23}) and R_{INT} (R_{10})

The IC is designed to operate with a minimum C_{23} capacitor of 4.7nF and a minimum C_2 (effective) = 10µF.

Note that, for high voltage A_{VDD}, the voltage coefficient of ceramic capacitors (C_2) reduces their effective capacitance greatly; a 16V 10µF ceramic can drop to around 3µF at 15V.

To improve the transient load response of A_{VDD} in PI mode, a resistor may be added in series with the C_{23} capacitor. The larger the resistor the lower the overshoot but at the expense of stability of the converter loop - especially at high currents.

With L = 10µH, A_{VDD} = 15V, C_{23} = 4.7nF, C_2 (effective) should have a capacitance of greater than 10µF. R_{INT} (R_7) can have values up to 5kΩ for C_2 (effective) up to 20µF and up to 10K for C_2 (effective) up to 30µF.

Larger values of R_{INT} (R_7) may be possible if maximum A_{VDD} load currents less than the current limit are used. To ensure A_{VDD} stability, the IC should be operated at the maximum desired current and then the transient load response of A_{VDD} should be used to determine the maximum value of R_{INT}.

Operation of the DELB Output Function

An open drain DELB output is provided to allow the boost output voltage, developed at C_2 (see application diagram), to be delayed via an external switch (Q4) to a time after the V_{BOOST} supply and negative V_{OFF} charge pump supply have achieved regulation during the start-up sequence shown in Figures 33 and 34. This then allows the A_{VDD} and V_{ON} supplies to start-up from 0V instead of the normal offset voltage of V_{IN}-V_{DIODE} (D_1) if Q4 were not present.

When DELB is activated by the start-up sequencer, it sinks 50µA allowing a controlled turn-on of Q4 and charge-up of C_9. C_{16} can be used to control the turn-on time of Q4 to reduce inrush current into C_9. The potential divider formed by R_9 and R_8 can be used to limit the V_{GS} voltage of Q4 if required by the voltage rating of this device. When the voltage at DELB falls to less than 0.6V, the sink current is increased to ~1.2mA to firmly pull DELB to 0V.

The voltage at DELB is monitored by the fault protection circuit so that if the initial 50µA sink current fails to pull DELB below ~0.6V after the start-up sequencing has completed, then a fault condition will be detected and a fault time-out ramp will be initiated on the C_{DEL} capacitor (C_7).

Operation of the PG Output Function

The PG output consists of an internal pull-up PMOS device to V_{IN}, to turn-off the external Q1 protection switch and a current limited pull-down NMOS device which sinks ~15µA allowing a controlled turn-on of Q1 gate capacitance. C_O is used to control how fast Q1 turns-on - limiting inrush current into C_1. When the voltage at the PG pin falls to less than 0.6V, the PG sink current is increased to ~1.2mA to firmly pull the pin to 0V.

The voltage at PG is monitored by the fault protection circuit so that if the initial 15µA sink current fails to pull PG below ~0.6V after the start-up sequencing has completed, then a fault condition will be detected and a fault time-out ramp will be initiated on the C_{DEL} capacitor (C_7).

Cascaded MOSFET Application

A 20V N-channel MOSFET is integrated in the boost regulator. For the applications where the output voltage is greater than 20V, an external cascaded MOSFET is needed as shown in Figure 27. The voltage rating of the external MOSFET should be greater than V_{BOOST}.

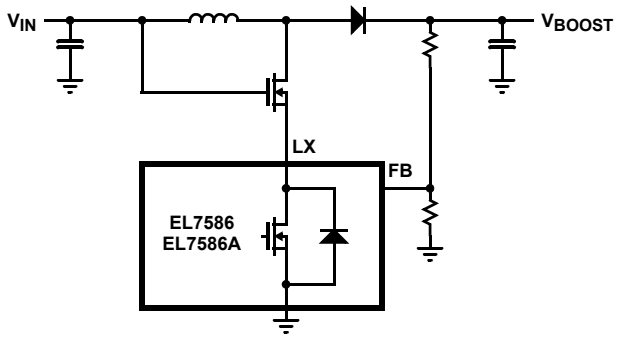


FIGURE 27. CASCADED MOSFET TOPOLOGY FOR HIGH OUTPUT VOLTAGE APPLICATIONS

Linear-Regulator Controllers (V_{ON}, V_{LOGIC}, and V_{OFF})

The EL7586 and EL7586A include three independent linear-regulator controllers, in which two are positive output voltage (V_{ON} and V_{LOGIC}), and one is negative. The V_{ON}, V_{OFF}, and V_{LOGIC} linear-regulator controller functional diagrams, applications circuits are shown in Figures 28, 29, and 30 respectively.

Calculation of the Linear Regulator Base-Emitter Resistors (R_{BL}, R_{BP} and R_{BN})

For the pass transistor of the linear regulator, low frequency gain (Hfe) and unity gain freq. (f_T) are usually specified in the datasheet. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/Hfe$. Therefore, in order to maintain phase margin at low frequency, the best choice for a pass device is often a high frequency low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor R_{BE} (R_{BP}, R_{BL}, R_{BN} in the Functional Block Diagram), which increase the pole frequency to: $f_p = f_T*(1+ Hfe *re/R_{BE})/Hfe$, where re = KT/qIc. So choose the lowest value R_{BE} in the design as long as there is still enough base current (I_B) to support the maximum output current (I_C).

We will take as an example the V_{LOGIC} linear regulator. If a Fairchild FMMT549 PNP transistor is used as the external pass transistor, Q5 in the application diagram, then for a maximum V_{LOGIC} operating requirement of 500mA the data sheet indicates Hfe_min = 100.

The base-emitter saturation voltage is: Vbe_max = 1.25V (note this is normally a Vbe ~ 0.7V, however, for the Q5 transistor an internal Darlington arrangement is used to increase it's current gain, giving a 'base-emitter' voltage of 2 x V_{BE}).

(Note that using a high current Darlington PNP transistor for Q5 requires that $V_{IN} > V_{LOGIC} + 2V$. Should a lower input voltage be required, then an ordinary high gain PNP transistor should be selected for Q5 so as to allow a lower collector-emitter saturation voltage).

For the EL7586 and EL7586A, the minimum drive current is:
I_DRVL_min = 8mA

The minimum base-emitter resistor, R_{BL}, can now be calculated as:

R_{BL}_min = V_{BE}_max/(I_DRVL_min - Ic/Hfe_min) = 1.25V/(8mA - 500mA/100) = 417Ω

This is the minimum value that can be used - so, we now choose a convenient value greater than this minimum value; say 500Ω. Larger values may be used to reduce quiescent current, however, regulation may be adversely affected, by supply noise if R_{BL} is made too high in value.

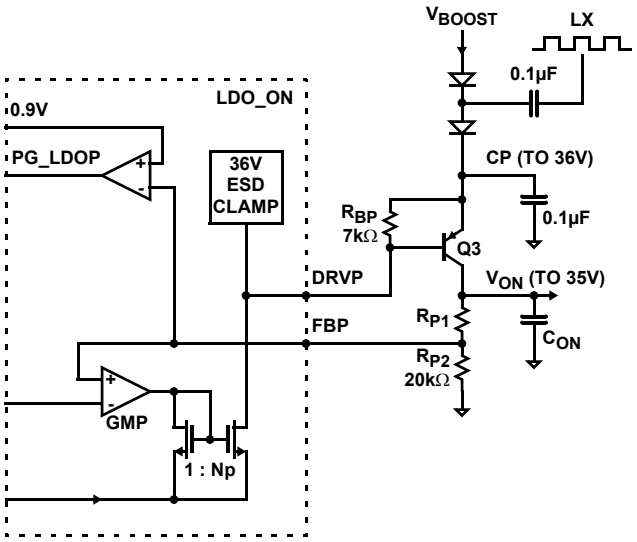


FIGURE 28. V_{ON} FUNCTIONAL BLOCK DIAGRAM

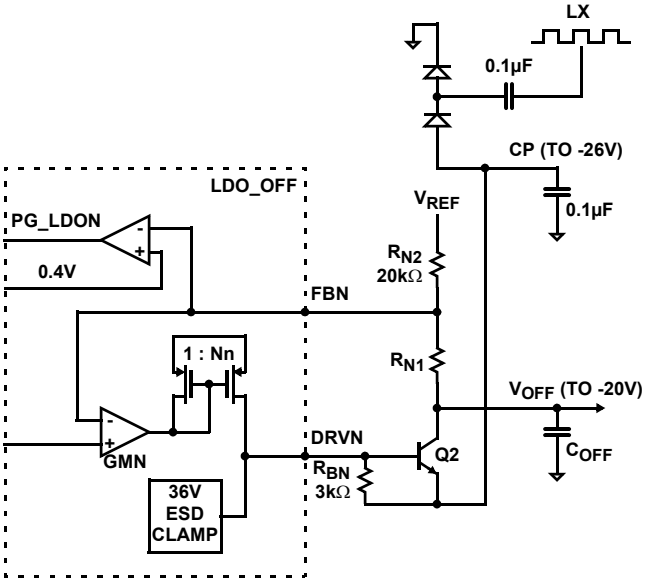


FIGURE 29. V_{OFF} FUNCTIONAL BLOCK DIAGRAM

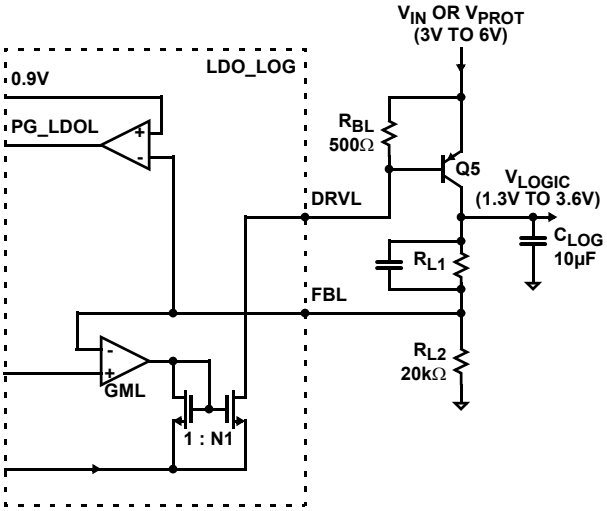


FIGURE 30. V_{LOGIC} FUNCTIONAL BLOCK DIAGRAM

The V_{ON} power supply is used to power the positive supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_ON). The LDO_ON regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{ON} voltage supported by EL7586 and EL7586A ranges from +15V to +36V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

The V_{OFF} power supply is used to power the negative supply of the row driver in the LCD panel. The DC/DC consists of an external diode-capacitor charge pump powered from the inductor (LX) of the boost converter, followed by a low dropout linear regulator (LDO_OFF). The LDO_OFF regulator uses an external NPN transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 4mA drive current, which is sufficient for up to 40mA or more output current under the low dropout condition (forced beta of 10). Typical V_{OFF} voltage supported by EL7586 and EL7586A ranges from -5V to -20V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 200mV above the 0.2V reference level.

The V_{LOGIC} power supply is used to power the logic circuitry within the LCD panel. The DC/DC may be powered directly from the low voltage input, 3.3V or 5.0V, or it may be powered through the fault protection switch. The LDO_LOGIC regulator uses an external PNP transistor as the pass element. The onboard LDO controller is a wide band (>10MHz) transconductance amplifier capable of 16mA drive current, which is sufficient for up to 160mA or

more output current under the low dropout condition (forced beta of 10). Typical V_{LOGIC} voltage supported by EL7586 and EL7586A ranges from +1.3V to V_{DD}-0.2V. A fault comparator is also included for monitoring the output voltage. The undervoltage threshold is set at 25% below the 1.2V reference.

Set-Up Output Voltage

Refer to the Typical Application Diagram, the output voltages of V_{ON}, V_{OFF}, and V_{LOGIC} are determined by the following equations:

$$V_{ON} = V_{REF} \times \left(1 + \frac{R_{12}}{R_{11}}\right)$$

$$V_{OFF} = V_{REFN} + \frac{R_{22}}{R_{21}} \times (V_{REFN} - V_{REF})$$

$$V_{LOGIC} = V_{REF} \times \left(1 + \frac{R_{42}}{R_{41}}\right)$$

Where V_{REF} = 1.2V, V_{REFN} = 0.2V.

Resistor networks in the order of 250kΩ, 120kΩ and 10kΩ are recommended for V_{ON}, V_{OFF} and V_{LOGIC}, respectively.

Charge Pump

To generate an output voltage higher than V_{BOOST}, single or multiple stages of charge pumps are needed. The number of stage is determined by the input and output voltage. For positive charge pump stages:

$$N_{POSITIVE} \geq \frac{V_{OUT} + V_{CE} - V_{INPUT}}{V_{INPUT} - 2 \times V_F}$$

where V_{CE} is the dropout voltage of the pass component of the linear regulator. It ranges from 0.3V to 1V depending on the transistor. V_F is the forward-voltage of the charge pump rectifier diode.

The number of negative charge pump stages is given by:

$$N_{NEGATIVE} \geq \frac{|V_{OUTPUT}| + V_{CE}}{V_{INPUT} - 2 \times V_F}$$

To achieve high efficiency and low material cost, the lowest number of charge pump stages which can meet the above requirements, is always preferred.

High Charge Pump Output Voltage (>36V) Applications

In the applications where the charge pump output voltage is over 36V, an external npn transistor need to be inserted into between DRVP pin and base of pass transistor Q3 as shown in Figure 31; or the linear regulator can control only one stage charge pump and regulate the final charge pump output as shown in Figure 32.

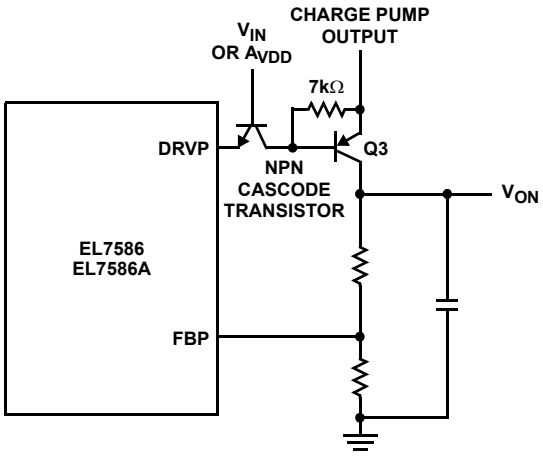


FIGURE 31. CASCODE NPN TRANSISTOR CONFIGURATION FOR HIGH CHARGE PUMP OUTPUT VOLTAGE (>36V)

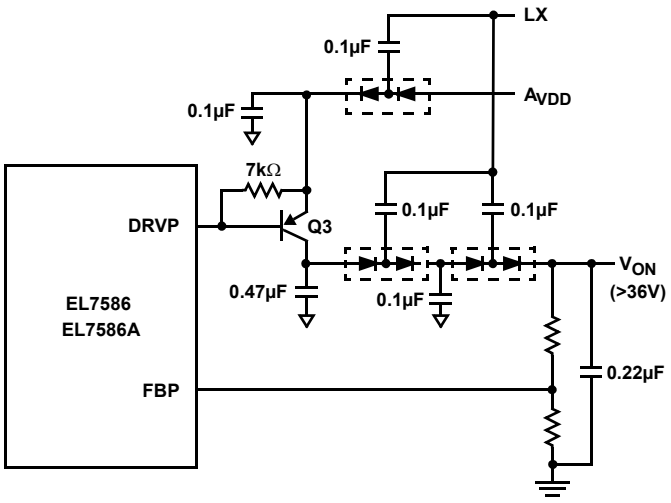


FIGURE 32. THE LINEAR REGULATOR CONTROLS ONE STAGE OF CHARGE PUMP

Discontinuous/Continuous Boost Operation and it's Effect on the Charge Pumps

The EL7586 and EL7586A V_{ON} and V_{OFF} architecture uses LX switching edges to drive diode charge pumps from which LDO regulators generate the V_{ON} and V_{OFF} supplies. It can be appreciated that should a regular supply of LX switching edges be interrupted, for example during discontinuous operation at light A_{VDD} boost load currents, then this may affect the performance of V_{ON} and V_{OFF} regulation - depending on their exact loading conditions at the time.

To optimize V_{ON}/V_{OFF} regulation, the boundary of discontinuous/continuous operation of the boost converter can be adjusted, by suitable choice of inductor given V_{IN}, V_{OUT}, switching frequency and the A_{VDD} current loading, to be in continuous operation.

The following equation gives the boundary between discontinuous and continuous boost operation. For continuous operation (LX switching every clock cycle) we require that:

$I(A_{VDD}\_load) > D*(1-D)*V_{IN}/(2*L*F_{OSC})$

where the duty cycle, $D = (A_{VDD} - V_{IN})/A_{VDD}$

For example, with V_{IN} = 5V, F_{OSC} = 1.0MHz and A_{VDD} = 12V we find continuous operation of the boost converter can be guaranteed for:

L = 10µH and $I(A_{VDD}) > 61mA$

L = 6.8µH and $I(A_{VDD}) > 89mA$

L = 3.3µH and $I(A_{VDD}) > 184mA$

Charge Pump Output Capacitors

Ceramic capacitors with low ESR are recommended. With ceramic capacitors, the output ripple voltage is dominated by the capacitance value. The capacitance value can be chosen by the following equation:

$$C_{OUT} \geq \frac{I_{OUT}}{2 \times V_{RIPPLE} \times f_{OSC}}$$

where f_{OSC} is the switching frequency.

Start-Up Sequence

Figure 33 and 34 show a detailed start-up sequence waveform. For a successful power up, there should be six peaks at V_{CDLY}. When a fault is detected, the device will latch off until either EN is toggled or the input supply is recycled.

When the input voltage is higher than 2.5V, an internal current source starts to charge C_{CDLY} to an upper threshold using a fast ramp followed by a slow ramp. During the initial slow ramp, the device checks whether there is a fault condition. If no fault is found, C_{CDLY} is discharged after the first peak and V_{REF} turns on.

During the second ramp, the device checks the status of V_{REF} and over temperature. At the peak of the second ramp, PG output goes low and enables the input protection PMOS Q1. Q1 is a controlled FET used to prevent in-rush current into V_{BOOST} before V_{BOOST} is enabled internally. Its rate of turn on is controlled by C_o. When a fault is detected, M1 will turn off and disconnect the inductor from V_{IN}.

With the input protection FET on, NODE1 (See Typical Application Diagram) will rise to ~V_{IN}. Initially the boost is not enabled so V_{BOOST} rises to V_{IN}-V_{DIODE} through the output diode. Hence, there is a step at V_{BOOST} during this part of the start-up sequence. If this step is not desirable, an external PMOS FET can be used to delay the output until the boost is enabled internally. The delayed output appears at A_{VDD}.

For the EL7586, V_{BOOST} and V_{LOGIC} soft-start at the beginning of the third ramp. The soft-start ramp depends on the value of the C_{DLY} capacitor. For C_{DLY} of 220nF, the soft-start time is ~2ms.

The EL7586A is the same as the EL7586 except V_{REF} and V_{LOGIC} turn on when input voltage (V_{DD}) exceeds 2.5V. When a fault is detected, the outputs and the input protection will turn off but V_{REF} will stay on.

V_{OFF} turns on at the start of the fourth peak. At the fifth peak, the open drain o/p DELB goes low to turn on the external PMOS Q4 to generate a delayed V_{BOOST} output.

V_{ON} is enabled at the beginning of the sixth ramp. A_{VDD}, PG, V_{OFF}, DELB and V_{ON} are checked at end of this ramp.

Fault Protection

Once the start-up sequence is complete, the voltage on the C_{DLY} capacitor remains at 1.15V until either a fault is detected or the EN pin is disabled. If a fault is detected, the voltage on C_{DLY} rises to 2.4V at which point the chip is disabled until the power is recycled or enable is toggled.

Component Selection for Start-Up Sequencing and Fault Protection

The C_{REF} capacitor is typically set at 220nF and is required to stabilize the V_{REF} output. The range of C_{REF} is from 22nF to 1µF and should not be more than five times the capacitor on C_{DEL} to ensure correct start-up operation.

The C_{DEL} capacitor is typically 220nF and has a usable range from 47nF minimum to several microfarads - only limited by the leakage in the capacitor reaching µA levels.

C_{DEL} should be at least 1/5 of the value of C_{REF} (See above). Note with 220nF on C_{DEL} the fault time-out will be typically 50ms and the use of a larger/smaller value will vary this time proportionally (e.g. 1µF will give a fault time-out period of typically 230ms).

Fault Sequencing

The EL7586 and EL7586A have advanced fault detection systems which protects the IC from both adjacent pin shorts during operation and shorts on the output supplies.

A high quality layout/design of the PCB, in respect of grounding quality and decoupling is necessary to avoid falsely triggering the fault detection scheme - especially during start-up. The user is directed to the layout guidelines and component selection sections to avoid problems during initial evaluation and prototype PCB generation.

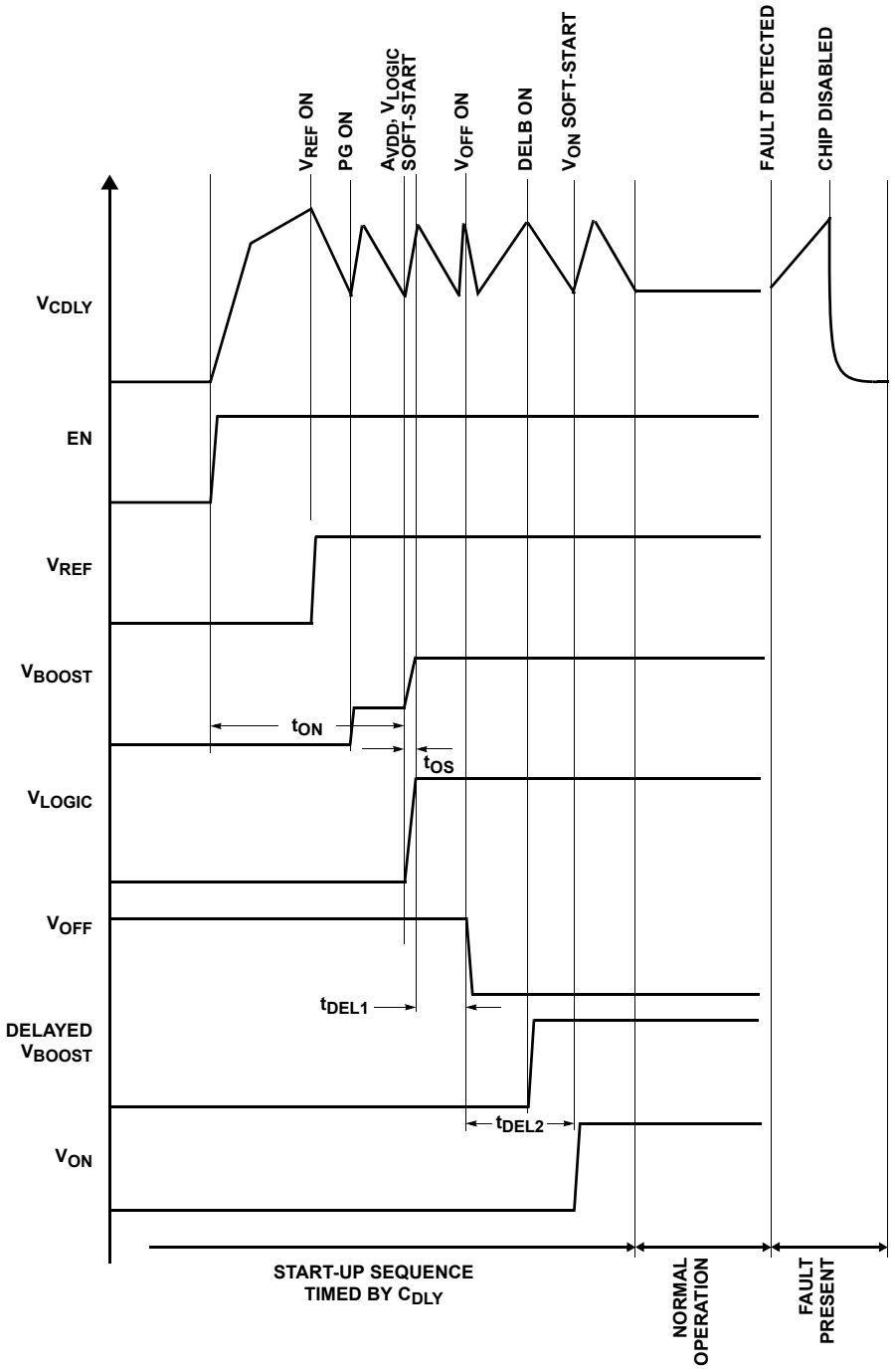


FIGURE 33. EL7586 START-UP SEQUENCE

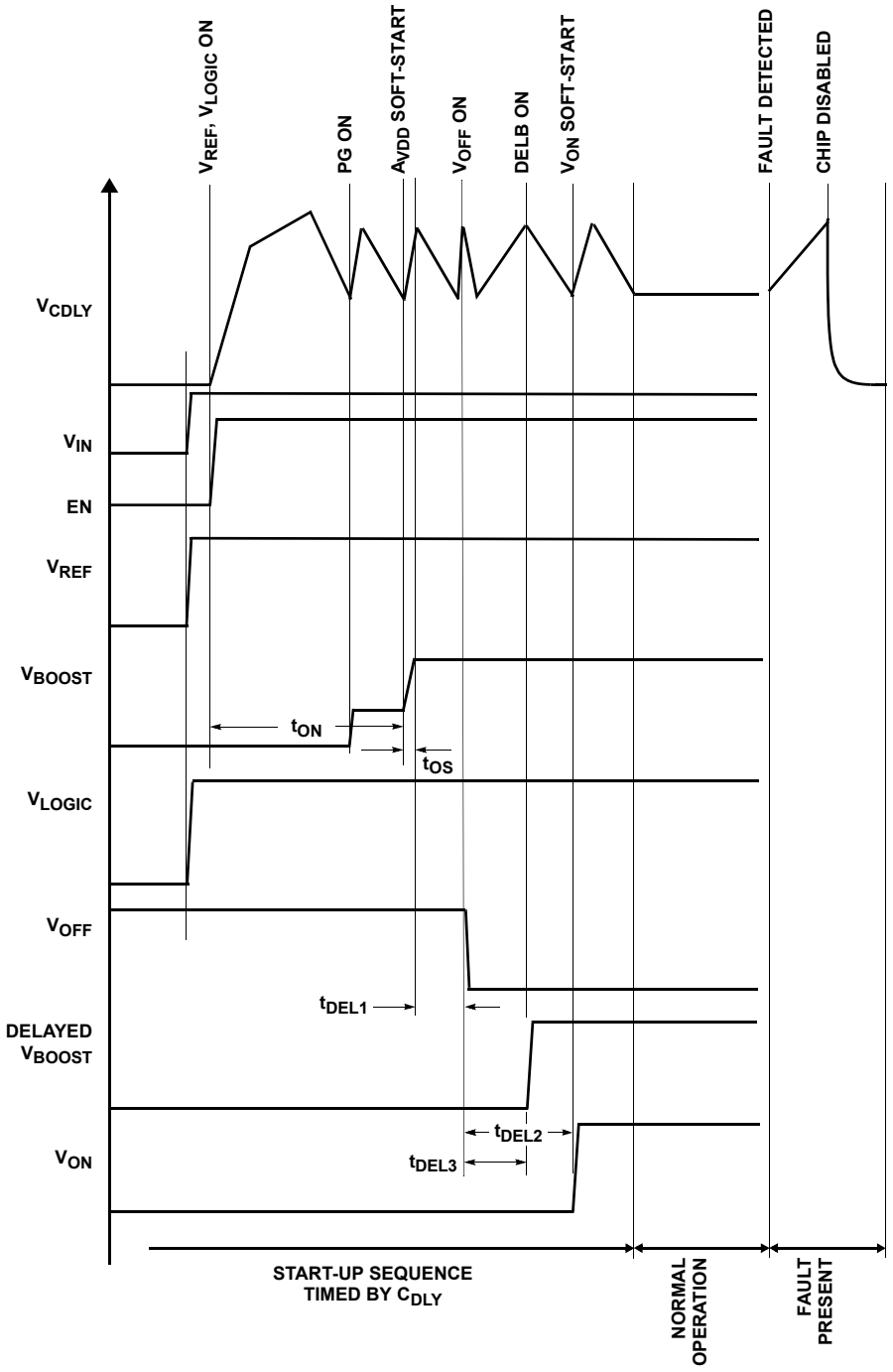


FIGURE 34. EL7586A START-UP SEQUENCE

Over-Temperature Protection

An internal temperature sensor continuously monitors the die temperature. In the event that the die temperature exceeds the thermal trip point of 140°C, the device will shut down.

Layout Recommendation

The device's performance including efficiency, output noise, transient response and control loop stability is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

There are some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{REF} and V_{DD} bypass capacitors close to the pins.
3. Minimize the length of traces carrying fast signals and high current.
4. All feedback networks should sense the output voltage directly from the point of load, and be as far away from LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at only one point near the main decoupling capacitors.
6. The exposed die plate, on the underneath of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize the thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. A signal ground plane, separate from the power ground plane and connected to the power ground pins only at the exposed die plate, should be used for ground return connections for feedback resistor networks (R_1, R_{11}, R_{41}) and the V_{REF} capacitor, C_{22}, the C_{DELAY} capacitor C_7 and the integrator capacitor C_{23}.
9. Minimize feedback input track lengths to avoid switching noise pick-up.

A demo board is available to illustrate the proper layout implementation.

Demo Board Layout

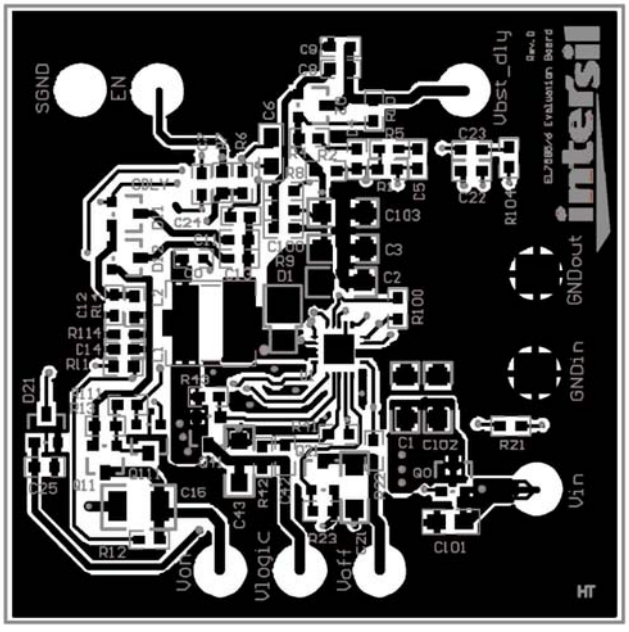


FIGURE 35. TOP LAYER

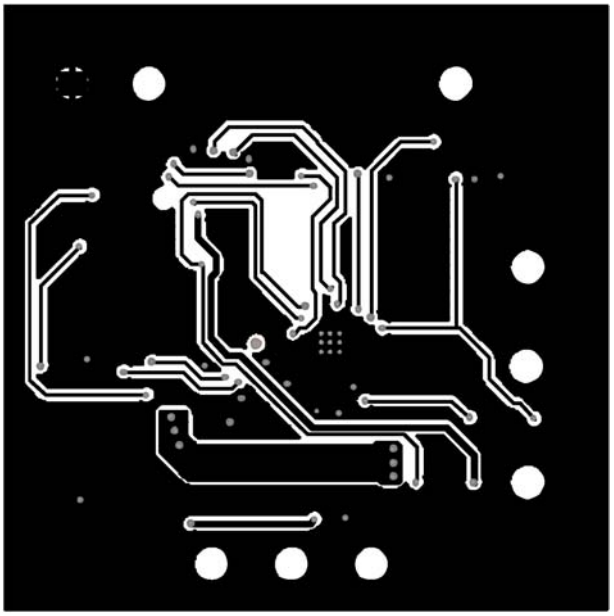
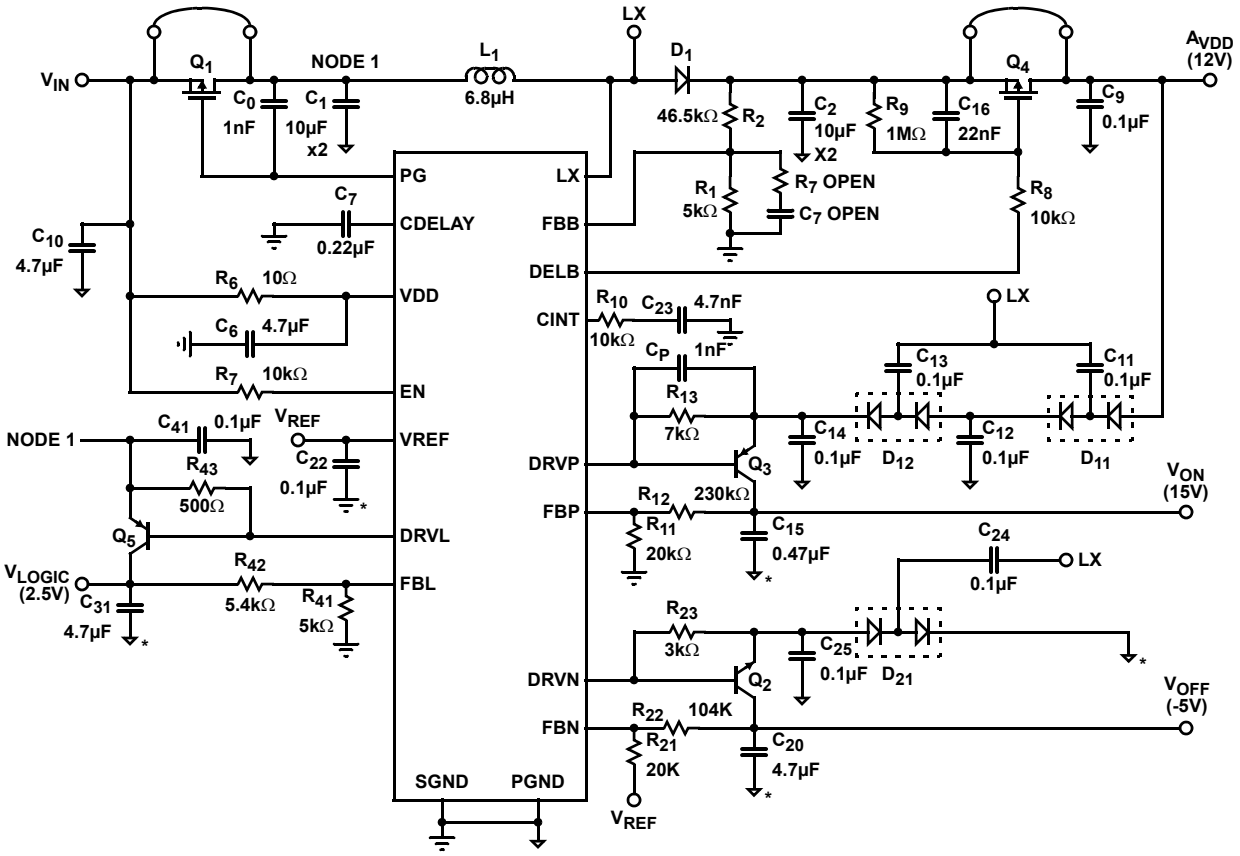


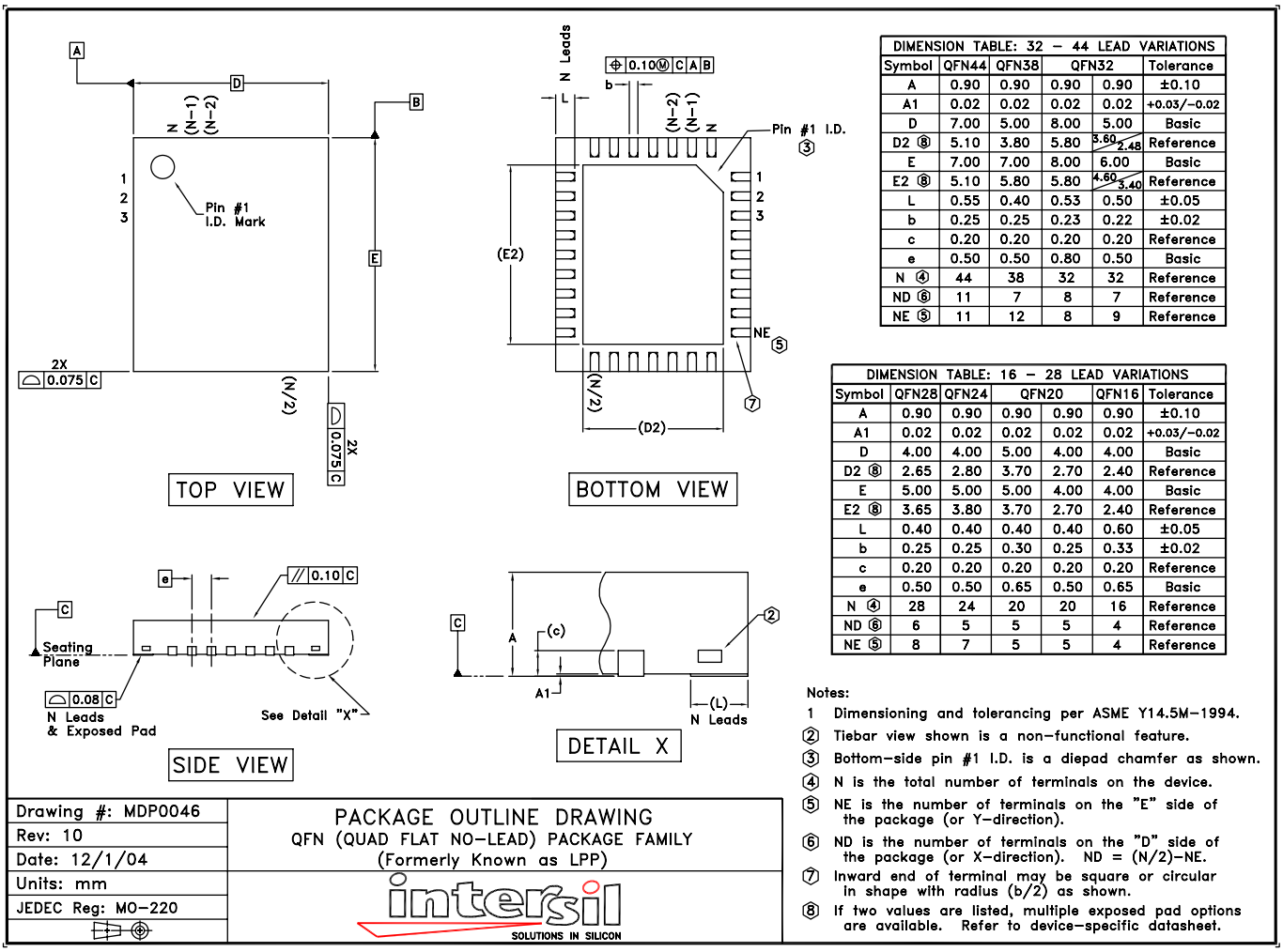
FIGURE 36. BOTTOM LAYER

Typical Application Diagram



NOTE: The SGND should be connected to the exposed die plate and connectd to the PGND at one point only.

QFN Package Outline Drawing



DIMENSION TABLE: 32 – 44 LEAD VARIATIONS					
Symbol	QFN44	QFN38	QFN32		Tolerance
A	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	+0.03/−0.02
D	7.00	5.00	8.00	5.00	Basic
D2 (8)	5.10	3.80	5.80	3.60 / 2.48	Reference
E	7.00	7.00	8.00	6.00	Basic
E2 (8)	5.10	5.80	5.80	4.60 / 3.40	Reference
L	0.55	0.40	0.53	0.50	±0.05
b	0.25	0.25	0.23	0.22	±0.02
c	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.80	0.50	Basic
N (4)	44	38	32	32	Reference
ND (6)	11	7	8	7	Reference
NE (5)	11	12	8	9	Reference

DIMENSION TABLE: 16 – 28 LEAD VARIATIONS						
Symbol	QFN28	QFN24	QFN20		QFN16	Tolerance
A	0.90	0.90	0.90	0.90	0.90	±0.10
A1	0.02	0.02	0.02	0.02	0.02	+0.03/−0.02
D	4.00	4.00	5.00	4.00	4.00	Basic
D2 (8)	2.65	2.80	3.70	2.70	2.40	Reference
E	5.00	5.00	5.00	4.00	4.00	Basic
E2 (8)	3.65	3.80	3.70	2.70	2.40	Reference
L	0.40	0.40	0.40	0.40	0.60	±0.05
b	0.25	0.25	0.30	0.25	0.33	±0.02
c	0.20	0.20	0.20	0.20	0.20	Reference
e	0.50	0.50	0.65	0.50	0.65	Basic
N (4)	28	24	20	20	16	Reference
ND (6)	6	5	5	5	4	Reference
NE (5)	8	7	5	5	4	Reference

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M–1994.
2. Tiebar view shown is a non–functional feature.
3. Bottom–side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the "E" side of the package (or Y–direction).
6. ND is the number of terminals on the "D" side of the package (or X–direction). ND = (N/2)–NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device–specific datasheet.

Drawing #: MDP0046	PACKAGE OUTLINE DRAWING
Rev: 10	QFN (QUAD FLAT NO–LEAD) PACKAGE FAMILY
Date: 12/1/04	(Formerly Known as LPP)
Units: mm	intersil SOLUTIONS IN SILICON
JEDEC Reg: MO–220	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp